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APPLICATION FOR LETTERS PATENT

for

STACKABLE CERAMIC FBGA FOR HIGH THERMAL APPLICATIONS

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TITLE OF THE INVENTION

STACKABLE CERAMIC FBGA FOR HIGH THERMAL APPLICATIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of application Serial No. 09/924,635, filed August 8, 2001, now U.S. Patent 6,650,007, issued November 18, 2003, which is a continuation of application Serial No. 09/344,279, filed June 30, 1999, now U.S. Patent 6,297,548, issued October 2, 2001, which claims the benefit of U.S. Provisional Application No. 60/091,205 filed June 30, 1998.

BACKGROUND OF THE INVENTION

[0002] Statement of the Invention: The present invention relates to an apparatus for high-temperature thermal applications for ball grid array semiconductor devices and a method of packaging ball grid array semiconductor devices.

[0003] State of the Art: Integrated semiconductor devices are typically constructed in wafer form with each device having the form of an integrated circuit die which is typically attached to a lead frame with gold wires. The die and lead frame are then encapsulated in a plastic or ceramic package, which is then commonly referred to as an integrated circuit (IC). ICs come in a variety of forms, such as a dynamic random access memory (DRAM), static random access memory (SRAM), read only memory (ROM), gate arrays, etc. The ICs are interconnected in many combinations on printed circuit boards by a number of techniques, such as socketing and soldering. Interconnection among ICs arrayed on a printed circuit board is typically made by conductive traces formed by photolithography and etching processes.

[0004] Such semiconductor devices typically take the form of the semiconductor die therein. The die is generally electrically attached to a lead frame within a package. The lead frame physically supports the die and provides electrical connections between the die and its operating environment. The die is generally electrically attached to the lead frame by means of fine gold wires. These fine gold wires function to connect the die to the lead frame so that the

gold wires are connected electrically in series with the lead frame leads. The lead frame and die are then encapsulated. The packaged chip is then able to be installed on a circuit board by any desired manner, such as soldering, socketing, etc.

[0005] However, as the speed of the semiconductor die increases, the heat generated during operation increases. Additionally, it becomes necessary to shorten the leads between the printed circuit board on which the IC is located and the IC device itself in order to keep the impedance of the circuit from affecting the response speed of the IC device.

[0006] The wires connecting the leads of the lead frame to the bond pads on the active surface of the semiconductor die in an IC package are not an effective connection for high operating speed semiconductor dice as the wires slow down the response of the semiconductor die.

[0007] Therefore, a packaging is required for semiconductor dice which have high operating speeds and generate heat associated therewith while minimizing the lead length between the semiconductor dice and the printed circuit boards on which they are mounted.

BRIEF SUMMARY OF THE INVENTION

[0008] The present invention comprises an apparatus package for high-temperature thermal applications for ball grid array semiconductor devices and a method of packaging ball grid array semiconductor devices.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0009] FIG. 1 is a cross-sectional view of a stack of a first embodiment of the packaged semiconductor dice of the present invention on a printed circuit board;

[0010] FIG. 2 is a top view of a packaged semiconductor die of the present invention;

[0011] FIG. 3 is a bottom view of a packaged semiconductor die of the present invention;

[0012] FIG. 4 is a cross-sectional view of stacks of the packaged semiconductor dice of the present invention on both sides of a printed circuit board;

[0013] FIG. 5 is a cross-sectional view of a stack of a second embodiment of the packaged semiconductor die of the present invention on a printed circuit board; and

[0014] FIG. 6 is a cross-sectional view of stacks of the second embodiment of the present invention on both sides of a printed circuit board.

[0015] The present invention will be better understood when the drawings are taken in conjunction with the description of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0016] Referring to drawing FIG. 1, a plurality of assemblies 10 comprising a carrier 12 and a semiconductor device 14 located therein is illustrated installed on a substrate 2. Each carrier 12 comprises a member having a cavity 16 therein. As illustrated, the cavity 16 may be a single-level or multi-level cavity having any desired number of levels therein. The carrier 12 is formed having a plurality of contact pads 18 located on the upper surface 20 and lower surface 22 thereof which is connected by circuits 24 (not shown) and by wire bonds 26 to the bond pads 28 located on the active surface 30 of the semiconductor die or device 14. The semiconductor die or device 14 is initially retained within the cavity 16 by any suitable means, such as adhesive, etc. The circuits 24 (not shown) are formed on the upper surface 20 of the carrier 12 and portions of the walls or surfaces of the cavity 16 by any suitable well-known means, such as deposition and etching processes. The wire bonds connecting the bond pads 28 of the semiconductor die or device 14 to the circuits 24 (not shown) are made using any suitable commercially available wire bonder. After the wire bonds 26 are formed, the cavity 16 is filled with suitable encapsulant material 32 covering and sealing the semiconductor die 14 in the cavity 16 and sealing the wire bonds 26 in position therein.

[0017] The carriers 12 may be of any desired geometric shape. The carrier 12 is formed having internal circuits 34 extending between the contact pads 18 on the upper surface 20 and lower surface 22 of the carrier 12. The carrier 12 is formed having frustoconical recess surfaces 36, lips 38, and frustoconical surfaces 40 on the upper surface 20. The surfaces 36 and 40 are formed having complementary angles so that the surfaces 36 and lips 38 of an adjacent carrier 12 mate or nest with an adjacent carrier 12 having surfaces 40 thereon, thereby forming a

stable, self-aligning stack of carriers 12. If desired, the carriers 12 may be formed having a plurality of heat transfer fins 42 thereon. The carrier 12 may be formed of any desired suitable material, such as ceramic material, high-temperature plastic material, etc. The carrier 12 may be formed by any suitable method, such as molding, extrusion, etc.

[0018] Once a plurality of carriers 12 having semiconductor die or devices 14 therein is formed as an assembly, the assembly is connected to the substrate 2 using a plurality of reflowed solder balls 50. The substrate 2 includes circuitry thereon, on either the upper surface or lower surface or both, and therein, as well as conductive vias, if desired. The substrate 2 may be any suitable substrate, such as a printed circuit board, FR-4 board, etc. Any desired number of carriers 12 may be stacked to form an assembly on the substrate 2. As illustrated, the reflowed solder balls 50 are located in alignment with the contact pads 18 and the connecting internal circuits 34 extending between the contact pads 18 on the upper surface 20 and lower surface 22 of a carrier 12.

[0019] Referring to drawing FIG. 2, a carrier 12 having circuits 24 thereon extending between contact pads 18 on the upper surface 20 of the carrier 12 is illustrated. For purposes of clarity, only a portion of the circuits 24 extending on the surface 20 of the carrier 12 is illustrated.

[0020] Referring to drawing FIG. 3, the bottom surface 22 of a carrier 12 is illustrated having a plurality of contact pads 18 located thereon.

[0021] Referring to drawing FIG. 4, a plurality of assemblies 10 is illustrated located on both sides of a substrate 2 being connected to the circuitry thereon by a plurality of reflowed solder balls 50.

[0022] Referring to drawing FIG. 5, a second embodiment of the present invention is illustrated. A plurality of assemblies 100 is stacked on a substrate 2, being electrically and mechanically connected thereto by reflowed solder balls 150. Each assembly 100 comprises a carrier 112 having a cavity 116 therein containing a semiconductor die or device 114 therein. The semiconductor die or device 114 is electrically connected to the circuits 134 of the carrier 112 by reflowed solder balls 126. Each carrier 112 is formed having apertures 160 therethrough connecting with circuits 134. Each carrier 112 is formed with surfaces 136 and 140 as well as lips 138 as described hereinbefore with respect to carrier 12. To connect each

carrier 112 to an adjacent carrier 112, a conductive material 162, such as conductive epoxy, solder, etc., is used to fill the apertures 160 in the carriers and contact the conductive material 162 in adjacent carriers 112.

[0023] The carriers 112 are similar in construction to the carriers 12 as described hereinbefore, except for the apertures 160, conductive material 162, circuits 134, and reflowed solder balls 126 between the semiconductor die or device 114 and the circuits 134.

[0024] The substrate 2 is the same as described hereinbefore.

[0025] Referring to drawing FIG. 6, a plurality of assemblies 100 is illustrated stacked on both sides of a substrate 2, being electrically and mechanically connected thereto by reflowed solder balls 150.

[0026] The present invention includes additions, deletions, modifications, and alterations which are within the scope of the claims.